<table>
<thead>
<tr>
<th>AMD 2013-2014 SERVER ROADMAP</th>
</tr>
</thead>
</table>

### 2P and 4P Enterprise, Mainstream Platforms

<table>
<thead>
<tr>
<th>Year</th>
<th>Product Line</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2013</strong></td>
<td>AMD Opteron™ 6300 and 4300 Series</td>
<td>4, 6, 8, 12 or 16 “Piledriver” CPU Cores 35W-140W</td>
</tr>
<tr>
<td><strong>2014</strong></td>
<td>“Warsaw” CPU</td>
<td>12 or 16 “Piledriver” CPU Cores</td>
</tr>
</tbody>
</table>

### 1P Web/Enterprise Services Clusters

<table>
<thead>
<tr>
<th>Year</th>
<th>Product Line</th>
<th>Features</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2013</strong></td>
<td>AMD Opteron™ 3300 Series</td>
<td>4 or 8 “Piledriver” CPU Cores 25W-65W TDP</td>
</tr>
<tr>
<td><strong>2014</strong></td>
<td>“Berlin” CPU/APU</td>
<td>4 “Steamroller” CPU Cores GCN Graphics Compute Units (APU) HSA Features (APU)</td>
</tr>
<tr>
<td><strong>2015</strong></td>
<td>AMD Opteron™ X1150 CPU and X2150 APU</td>
<td>4 “Jaguar” CPU Cores GCN Graphics Compute Units (APU) 9W-22W</td>
</tr>
<tr>
<td><strong>2016</strong></td>
<td>“Seattle” CPU</td>
<td>ARM “A57” CPU Cores</td>
</tr>
</tbody>
</table>

**Notes:** AMD roadmaps are subject to change without notice or obligations to notify of changes. Placement of boxes intended to represent first year of production shipments.
A History of Energy Efficiency

ENERGY EFFICIENCY (LOG SCALE)

2008 2009 2010 2011 2012 2013 2014

“Puma” “Tigris” “Danube” “Trinity” “Llano” “Richland” “Kaveri” 10X

Dynamic power tracking and management with DVFS
Finer grained power tracking, increased voltage granularity
Integrated voltage regulation

Thermal aware power management
Dynamic thermal tracking for short term boost
Platform aware dynamic thermal management

Video decode acceleration
Video encode acceleration
Audio acceleration
Inter-frame power gating

Finer grained voltage planes
Fine grained power gating
Voltage-adaptive frequency scaling
Per part adaptive voltage

ACPI driven workload specific optimization
Dynamic CPU ↔ GPU power sharing
Intelligent boost and Performance aware energy optimization

Power efficient APU architecture integrating GPU+CPU and accelerators
OpenCL GPU compute moving to full HSA enabled programming

In market  In product  In development
Power consumption (and hence performance) is set by the cooling capabilities of the platform.

Power varies a lot by workload.

We measure and manage the power of each component on the chip to generate the best performance/watt.
To manage temperature and send the power wherever it’s needed, we use power monitors in all chip components.

“Kyoto” has power monitors in each CPU, the GPU, the display interface, and the FCH.

The central controller uses this information to optimize performance within thermal constraints.
<table>
<thead>
<tr>
<th>Year</th>
<th>Processor</th>
<th>Boosting decision based on</th>
<th>Notes</th>
</tr>
</thead>
</table>
| 2010 | AMD Phenom™ II | - Number of cores active | - **Single boost Pstate** used if half or more cores are inactive  
- Coarse-grain power margin exploited |
| 2011 | 1st-Generation AMD A-Series APU | - Calculated power | - **Unidirectional power transfer** between thermal entities  
- GPU→CPU  
- Exploit fine-grain power margin |
| 2012 | 2nd-Generation AMD A-Series APU | - Calculated power  
- Calculated temperature | - **Bidirectional power transfer** between thermal entities  
- GPU→CPU  
- CPU→GPU  
- Exploit temperature margin |
| 2013 | 3rd-Generation AMD A-Series APU ("Richland") | - Calculated power  
- Calculated temperature  
- Measured/Sensor temperature  
- Efficiency of power usage by individual entities (CPU, GPU, etc.) | - Designed to more effectively exploit temperature margin by detecting favorable thermal conditions in real time  
- Intelligent Boost |
CHIP-LEVEL POWER DISTRIBUTIONS: GPU-CENTRIC

Lower-power cores serve as a heat sink for the active GPU.
CHIP-LEVEL POWER DISTRIBUTIONS: CPU-CENTRIC

Kabini Temperature

Lower-power GPU serves as a heat sink for the active CPUs
Avoiding power waste with Intelligent Boost control

- Intelligent Boost is designed to avoid power waste that results from boosting applications that benefit very little from higher frequency.
- Enables long battery life and cool operation while maintaining great performance.
- Power management microcontroller tracks application behavior real-time to determine frequency sensitivity.
- Boost behavior is adjusted accordingly.

Performance metrics tracked by power manager:

- Frequency Sensitivity (i.e., % perf gain for % freq gain)

Different applications:

- BOOST THESE
- DON’T BOOST THESE
FABRICS REDUCE THE POWER CONSUMPTION OF EVERY SERVER

- ~70% of energy consumption in servers from components beyond CPU
- Eliminate unnecessary components and functions
- Remove tiers of networking equipment and thousands of cables

**BENEFITS**

- **SHARE**
  - Sharing instead of replicating components eliminates pieces from motherboard
  - Reduces power and space

- **POWER OPTIMIZE**
  - Turning off unneeded logic blocks saves power

- **LINK EFFICIENT UNITS**
  - A low cost, on board interconnect allows removal of top of rack switching and increases bandwidth
Slide Sources

- “Richland” Client APU” Presentation by Praveen Dongara, Lloyd Bircher, John Darrilek - Hot Chips 25, August 2013
- “AMD Product and Tech Roadmaps 5.5.14”
- “Energy Efficiency” by Sam Naffziger, June 16, 2014
- “AMD “Kabini” APU SOC” by Dan Bouvier, Ben Bates, Walter Fry, Sreekanth Godey – Hot Chips 25, August 2013
- “Energy Efficiency Messaging” May 9, 2014
- “AMD Advanced Power Management” by Sam Naffziger, April 2014
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